CLAIMS

1. (Withdrawn) An apparatus comprising:

a device structure having a first metal layer:

an electrically decoupling capacitor stack coupled to the first metal layer having a top electrode wherein the top electrode is coupled through a via a second metal layer superimposed over a portion of the first metal layer; and

an interlayer dielectric layer coupled between the first metal layer and the second metal layer, wherein the interlayer dielectric comprises alternating layers of dissimilar dielectric material defining vertical corrugations in a wall of the via,

wherein the decoupling capacitor stack conforms to the vertical corrugations.

2. (Withdrawn) The apparatus of claim 2, wherein the interlayer dielectric comprises alternating layers of silicon nitride and silicon oxide.

3. (Withdrawn) The apparatus of claim 1, wherein the decoupling capacitor stack contacts the first metal layer, the vertical corrugations in the via wall and a top portion of the interlayer dielectric layer in an area adjacent to the via.

4. (Withdrawn) The apparatus of claim 1, wherein the corrugated decoupling capacitor structure is supported by alternating layers of via metal material having dissimilar etch rates.

5. (Withdrawn) The apparatus of claim 4, wherein the alternating layers of via metal material comprise a metal and a metal nitride system.

6. (Withdrawn) The apparatus of claim 5, wherein the metal comprises one of tantalum, titanium and tungsten.

7. (Original) A method comprising:

forming an interlayer dielectric comprising alternating layers of dissimilar dielectric materials in a multilayer stack over a metal layer of a device structure;

forming a via having a corrugated sidewall; and

forming a decoupling capacitor stack in the via that conforms to the sidewall of the via.

8. (Original) The method of claim 7, further comprising:

forming the interlayer dielectric layer by depositing alternating layers of dielectric material of different etch selectivities.

9. (Original) The method of claim 8, further comprising:

forming the via using an etch chemistry having an anisotropic etch characteristic toward one of alternative layers of dielectric material.

10. (Original) The method of claim 7, further comprising:

forming the via by etching the via with a wet HF etch to form the corrugated vertical surfaces.

11. (Original) The method of claim 7, further comprising:

depositing the decoupling capacitor stack in the via that conforms to the vertical corrugations of the via by atomic layer chemical vapor deposition.

12. (Original) A method comprising:

forming a multilayer interlayer dielectric on an integrated circuit having a metal layer;

etching a via in the multilayer interlayer dielectric;

etching corrugations in a surface of the via in the multilayer interlayer dielectric;

depositing a decoupling capacitor on the surface of the via that conforms to the corrugations in the surface of the via;

filling the via with a via metal that conforms to the corrugations in the decoupling capacitor; and

forming a metal layer over the via and interlayer dielectric.

13. (Original) The method of claim 12, further comprising:

forming a multilayer interlayer dielectric by altering the chemistry of a physical vapor deposition tool to alternate between depositing a first dielectric material and a second dielectric material.

14. (Original) The method of claim 12, further comprising:

depositing the conformal decoupling capacitor by atomic layer chemical vapor deposition.

15. (Original) The method of claim 14, further comprising:

depositing a conformal top and bottom capacitor electrode by atomic layer chemical vapor deposition of alternating layers of titanium and nitrogen.

16. (Original) The method of claim 14, further comprising:

depositing a conformal dielectric capacitor layer by atomic layer chemical vapor deposition of alternating layers of tantalum and oxygen.